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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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HIDALGO, FERNANDO N	
ART UNIT	**PAPER NUMBER**
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/586,176	KOHLER ET AL.	
	Examiner	Art Unit	
	FERNANDO N. HIDALGO	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 7-15, 17-31* is/are rejected.

7)☒ Claim(s) *6 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/27/09*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments substantially with respect to independent claim(s) 1, 11, 21, 24 and 27 have been considered but are moot in view of the new ground(s) of rejection. Furthermore, the Appeal Brief, as filed on 7/31/09, is moot in view of the new grounds of rejection as set forth below.

Allowable Subject Matter

2. **Claim(s) 6 and 16** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

3. The following is a statement of reasons for the indication of allowable subject matter: the pertinent prior art of record does not teach or suggest, in combination with intervening claim limitations, the steps of' raising a source terminal for each of said array of transistors to a positive potential; raising a gate terminal for all transistors along a selected mw to a positive potential and detecting whether a drain voltage changes from a precharge voltage level to approximately a cell transistor threshold voltage below said positive gate terminal potential.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claim(s) 1-5, 7-15, 17-23 and 27-31** are rejected under 35 U.S.C. 103(a) as being unpatentable over WO 2004/053889 A1 to Reiner ("Reiner") in view of U.S. Patent 6909635 B2 to Forbes et al. ("Forbes") and U.S. Publication Charging and discharging properties of electron traps created by hot-carrier injection in gate oxide on n-channel metal oxide semiconductor field effect transistor to Vuillaume et al. ("Vuillaume").

As to claim 1-2, Reiner teaches a method for programming a one time programmable memory (See Abstract), comprising the steps of obtaining an array of transistors (Page 7, lines 12-13); and programming at least one of said transistors using a hot carrier transistor aging technique to alter a characteristic of said at least one of said transistor (FIG. 1 shows memory transistor T2; Page 5, lines 19-page 6, down to line 19 disclose thermally damaging the drain junction of T2 by inducing hot carriers at the drain/oxide/gate junction), wherein the hot carrier aging technique comprises injection of carriers into a gate oxide (Page 7, lines 7-11 disclose gate oxide breakdown as induced by hot carriers resulting from T2 being voltage/current biased as disclosed on pages 5-6).

Complementary, Forbes teaches programming a OTP memory (At least paragraphs [0005-0006]), comprising the steps of: obtaining an array of transistors (As well known in the art: memories comprise arrays and evidence of this teaching is found in at least paragraphs [0003-004], [0057-0061]); and programming at least one of said transistors using a hot carrier transistor aging

technique to alter a characteristic of said at least one of said transistor, wherein the hot carrier aging technique comprises injection of carriers into a gate oxide, and wherein the injection of carriers causes at least one of, the creation of traps, and the filling of traps (At least paragraphs [0011], [0015], [0027], [0028], [0031], [0032-0036], [0038-0045]).

Forbes, furthermore, teaches applying a stressful voltage to said at least one transistor to cause said hot carrier transistor aging (At least paragraph 0037] and FIG. 2B).

Furthermore, Vuillaume teaches the fundamental technology aspects of electron traps created by hot-carrier injections in gate oxides of semiconductor transistors; particularly, but not limitedly, the evidence is presented of "creation of acceptor-like traps ... It has been shown that these ... traps are strongly localized above the drain in the oxide of the gat-drain overlap region of the MOSFET," in at least section I, but not limited thereto, of Vuillaume.

Reiner, Forbes and Villaume are analogous art because they are from the same filed of endeavor regarding semiconductor circuit design, in particular transistors having hot carrier induced effects.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to incorporate teachings of injection of carriers causes at least one of, the creation of traps, and the filling of traps as found in the teachings of Forbes and fundamental teachings of electron traps created by hot-carrier injections in gate oxide of MOSFETS in the teachings of Villaume. The

suggestion/motivation would have been obvious to one of ordinary skill in the art to conclude that injection of carriers, as induced by voltage/current biasing of a transistor device can cause oxide degradation resulting in charge trapping.

Therefore, it would have been obvious to combine Reiner with Forbes and Villaume to make the above modification.

As to claim 3, Reiner teaches said altered characteristic is a change in a threshold voltage of' said at least one of' said transistors (Page 6, lines 27-31 teach that T2 of FIG. 1, when not programmed in a reading operation, will not conduct current; yet when T2 is programmed, in contrast, it will conduct current, obviously changing the threshold voltage of the memory T2).

Furthermore, Forbes complements teachings of threshold changing (At least Abstract and [0011]).

As to claim 4, Reiner teaches said programming step further comprising the step of applying a stressful voltage to a drain and a gate of said at least one of said transistors to cause said change in said threshold voltage of' said of said at least one of' said transistors (Page 5, lines 7-page 6, down to line 7).

As to claim 5, Reiner teaches the step of detecting said programmed at least one of' said transistor by sensing said change in said threshold voltage of said at least one of said transistors (Page 6, lines 27-page 7, down to line 6 teach detecting current of a programmed memory T2 and a non-programmed memory, the current conduction changing accordingly, and therefore detecting

change in the threshold voltage which as well known is directly proportional to the conductive current of the memory transistor T2).

As to claim 7, Reiner teaches that said altered characteristic is a change in a saturation current of said at least one of said transistors (Page 6, lines 27-page 7, down to line 6 teach a change of current of programmed memory transistor T2 in FIG. 1 in comparison to a non-programmed memory transistor).

As to claim 8, Reiner teaches said programming step further comprising the step of applying a stressful voltage to a source and a gate of' said at least one of said transistor to cause said change in said saturation current of said of said at least one of' said transistors (Pages 5-6 teach programming of cell T2 in FIG. 1 hot-carrier stressing the drain terminal; as is well known, a source terminal is identical in functionality to a drain terminal in a MOS transistor, as such programming the source terminal follows the same teachings).

As to claim 9, Reiner teaches the step of detecting said programmed at least one of said transistors by sensing said change in said saturation current of said at least one of' said transistors (Page 6-7 teach detecting in a reading operation of the change in current of a programmed memory T2 in contrast to a non-programmed memory transistor).

As to claim 10, Reiner teaches said detecting step further comprises the steps of raising the voltage on at least one column in said array of transistors to a positive potential; raising a gate terminal of each transistor in a selected row to a positive potential and evaluating a rate of' voltage decay of at least one column in

said array of transistors (Page 6, line 22-23 teach raising a bit (column) line voltage to Vop while in a reading operation and detecting the current level change (voltage level change since Voltage is directly proportional to Current: V=(load)*I, where I is current, as well known)).

As to claim 11-12, see rejection to claims 1-2; furthermore a circuit (readout means) for sensing altered characteristics of said at least one of said transistors is taught on page 6, line 20-21.

As to claim 13, see rejection to claim 3.

As to claim 14, see rejection to claim 4.

As to claim 15, see rejection to claim 5.

As to claim 17, see rejection to claim 7.

As to claim 18, see rejection to claim 8.

As to claim 19, see rejection to claim 9.

As to claim 20, see rejection to claim 10.

As to claim 21, see rejection to claim 1-2; furthermore the teachings of Reiner and Forbes are in the context of an OTP (See at least page 1, lines 6-8 in Reiner; and at least paragraph [0006] in Forbes).

As to claim 22, see rejection to claim 7.

As to claim 23, see rejection to claim 3.

As to claim(s) 27-28, see rejection to claim 11-12.

As to claim 29, see rejection to claim 13.

As to claim 30, see rejection to claim 15.

As to claim 31, see rejection to claim 7.

6. **Claim(s) 24** is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Publication No. 2004/0027877 A1 to Kotz et al. ("Kotz") in view of U.S. patent No. 6888749 B2 to Forbes-2.

As to claim 24, Kotz teaches a memory cell, comprising only one transistor, wherein said transistor comprises: a source region; a drain region; a channel region; one silicon-dioxide gate insulator layer; and one gate electrode layer (At least paragraph [0022] teaches an OTP contains "only a single field-effect transistor" as illustrated in at least FIG. 1, wherein source/drain are 10/12, channel region is 22, oxide is 18, gate is 20).

While Kotz teaches of the oxide as silicon oxide (At least [0052]), it does not expressly submit "silicon-dioxide." However, silicon oxide and silicon -dioxide are well known in the art. Evidence of this teaching is found in at least Column 1, lines 5-6).

Kotz and Forbes-2 are analogous art because they are from the same filed of endeavor regarding semiconductor circuit design, in particular transistors having a gate oxide.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to incorporate teachings of a silicon-dioxide of Forbes-2. The suggestion/motivation would have been obvious to one of ordinary skill in the

art: a dielectric used between the gate and the channel, that is a gate oxide is formed, as well known, of silicon oxide (silicon -dioxide)..

Therefore, it would have been obvious to combine Kotz with Forbes-2 to make the above modification.

7. **Claim(s) 25-26** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Publication No. 2004/0027877 A1 to Kotz et al. ("Kotz") in view of U.S. patent No. 6888749 B2 to Forbes-2, and further in view of WO 2004/053889 A1 to Reiner ("Reiner") in view of U.S. Patent 6909635 B2 to Forbes et al. ("Forbes") and U.S. Publication Charging and discharging properties of electron traps created by hot-carrier injection in gate oxide on n-channel metal oxide semiconductor field effect transistor to Vuillaume et al. ("Vuillaume").

As to claim 25, see rejection to claim 1-2.

As to claim 26, Reiner teaches a plurality of said memory cells arranged in an array of rows and columns (Column 7, lines 12-13 teach an array of memory cells T2 of FIG. 1; an array of a memory is an arrangement of rows and columns of memory cells as well known; further, Merriam-Webster Dictionary defines array as elements arranged in rows and columns).

As to claim(s) 27-28, see rejection to claim 11-12.

As to claim 29, see rejection to claim 13.

As to claim 30, see rejection to claim 15.

As to claim 31, see rejection to claim 7.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FERNANDO N. HIDALGO whose telephone number is (571)270-3306. The examiner can normally be reached on Monday-Friday, 7:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Fernando N. Hidalgo/
Examiner, Art Unit 2827
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